

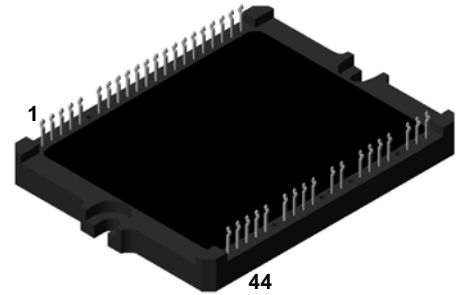
IPM with Sustain and Recovery driving function  
 Of electric power for PDP application

**Features**

- Trench IGBT
- Dip silicone molding structure
- Operating frequencies are optimized for 250kHz

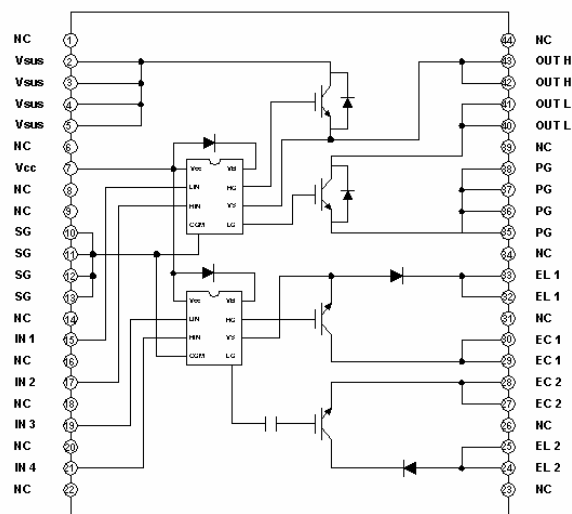
**Applications**

- Plasma Display Panel ( PDP )


**PACKAGE**
**Absolute Maximum Ratings @ Tc=25°C**

Symbol	Parameter	Condition	Ratings	Unit
Vce1	Collector to Emitter Voltage	Between pins 2 to 5 and pins 42,43 Between pins 40,41 and pins 35 to 38	300	V
Vce2	Collector to Emitter Voltage	Between pins 24,25 and pins 27,28 Between pins 29,30 and pins 32,33	270	V
Ic1	Collector peak Current (sustain and ground)	Pins 2 to 5, Pins 40,41 ①	400	A
Ic2	Collector peak Current (ERC rising and falling)	Pins 24,25, Pins 29,30 ①	200	A
Vrrm	Peak reverse Voltage	Between pins 27,28 and pins 24,25 Between pins 32,33 and pins 29,30	300	V
Vcc	Driver Power Supply	Pin 7	-0.3 to 25	V
VIN	Driver Input Voltage	Pins 15,17,19,21	-0.3 to Vcc+0.3	V
Tj	Operating junction temperature		-10 to +105	°C
Tstg	Storage temperature		-30 to +125	°C

**Note.** ① duty cycle=0.01, ton≤10usec

**Internal Equivalent Circuit**


**Recommended Operating Conditions @ Tc=25°C**

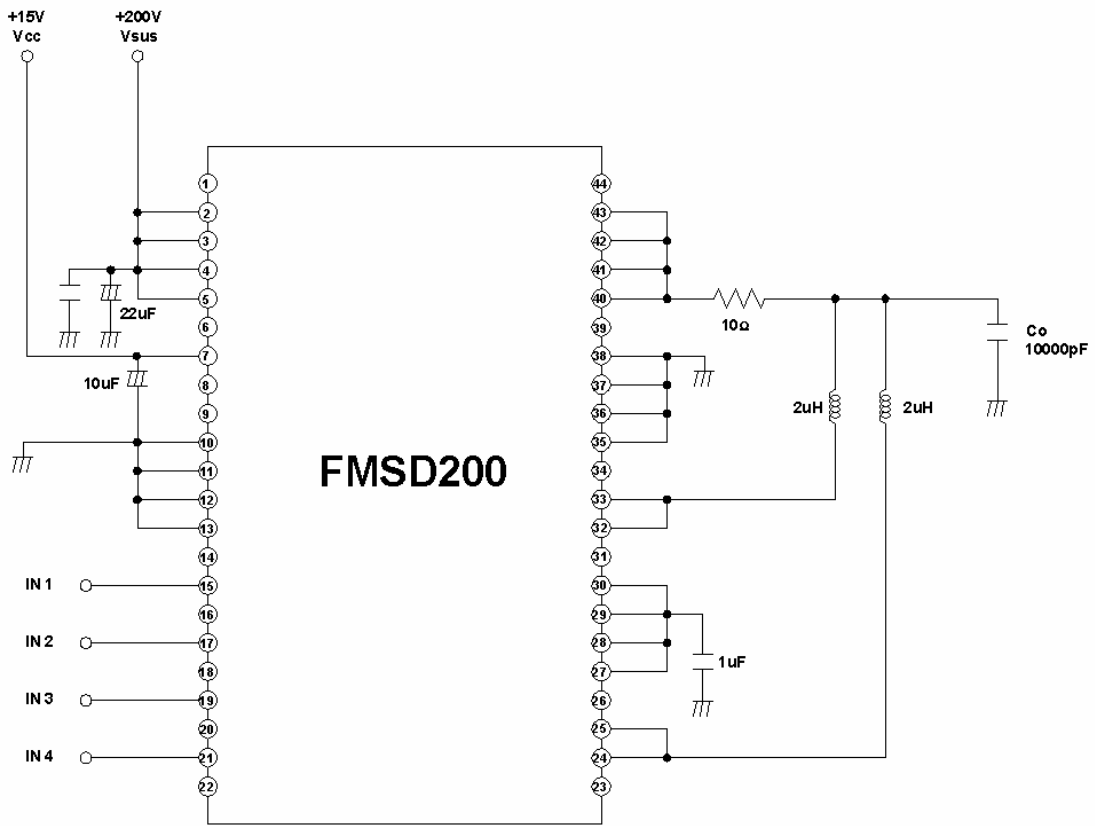
Symbol	Parameters	Condition	Ratings	Unit
Vcc	Driver Power supply voltage	Pin7	15	V
VIN	Driver Logic Input voltage	Pins 15, 17, 19, 21	0 to 5	V

**Electrical Characteristics @ Tc = 25°C (unless otherwise specified)**

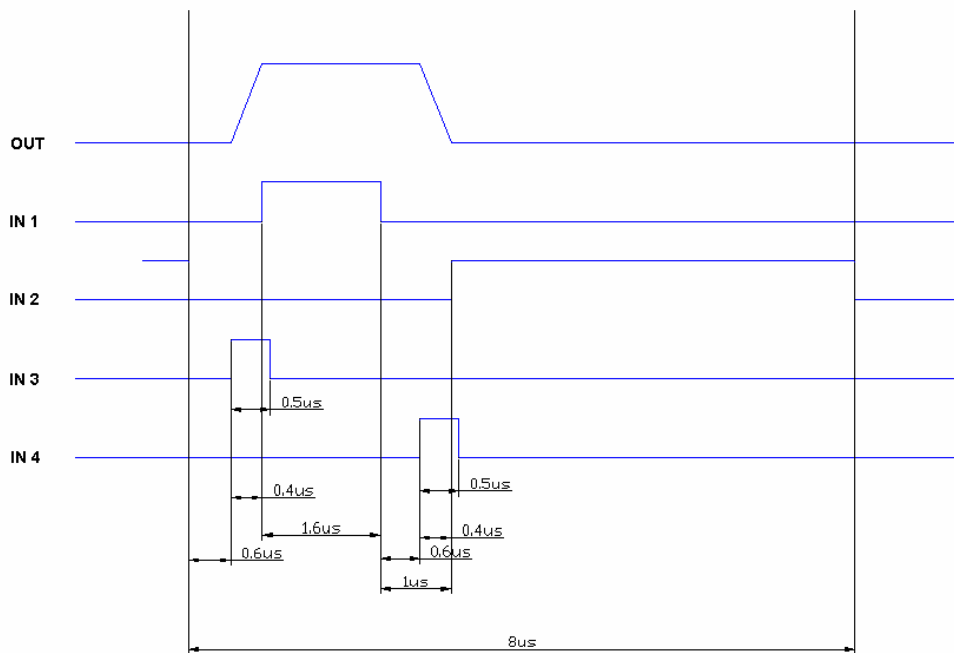
- Tc=25°C, Vsus=200V, Vcc=15V, Co=10000pF ( Test Circuit 1 )
- Tc=25°C, VCE = 40V, Vcc=15V, RL=8Ω or 470Ω or 20Ω ( Test Circuti 2, 3 )

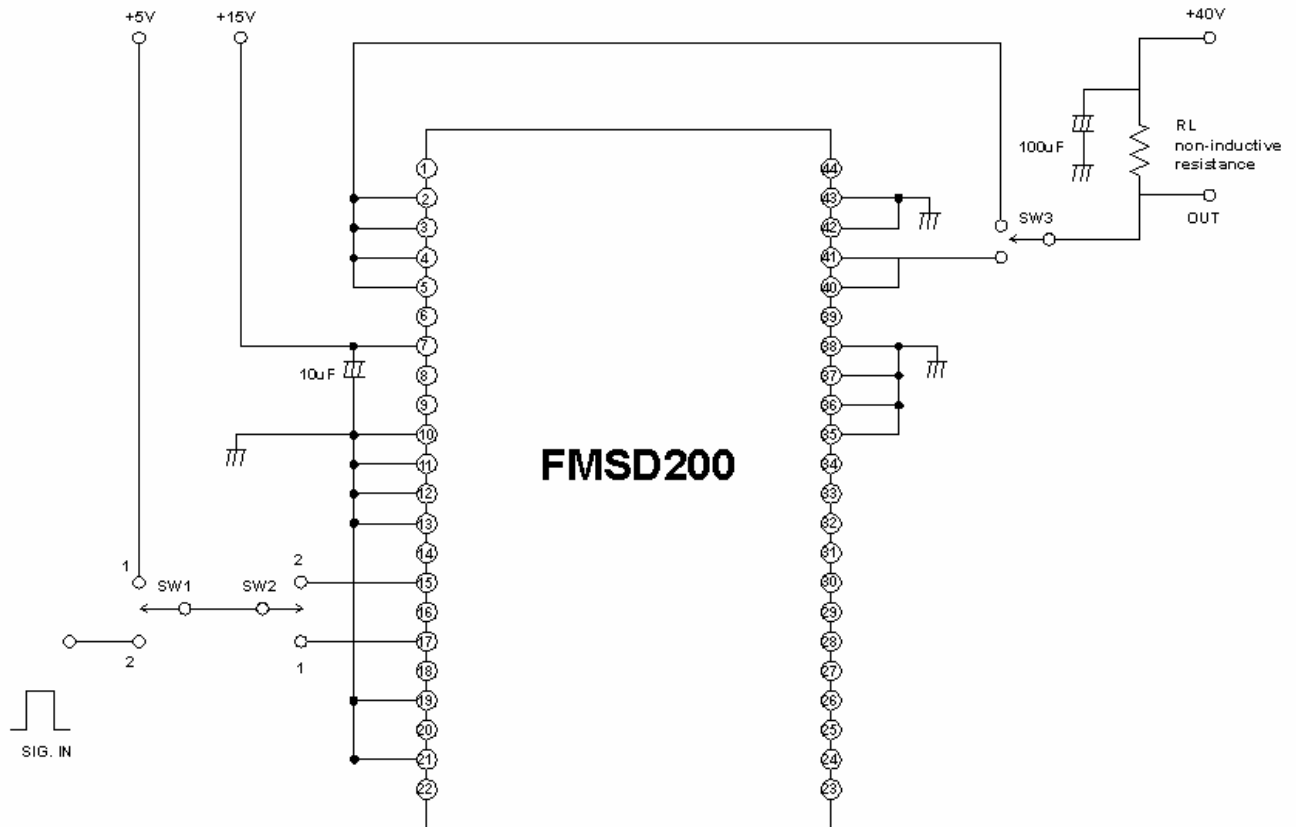
Symbol	Parameters	Test condition	Min	Typ	Max	Unit
VIH	Driver Input High level Voltage	Each pins 15,17,19,21	2.9	-	-	V
VIL	Driver Input Low level Voltage	Each pins 15,17,19,21	-	-	0.8	V
Icc	Driver Power supply Current	Pin 7, Vcc=15V, Test circuit 1	40		70	mA
VCE(SAT)	Collector to Emitter saturation Voltage	Between pins 2 to 5 And pins 42,43 Between pins 40,41 And pins 35 to 38			1.5-	V
ISUS	Collector to Emitter saturation Current	Pins 2 to 5	25		45	mA
ton1	Turn On Delay Time	Pin17 → Pins 42,43	140	-	280	ns
ton2		Pin15 → Pins 40,41				
ton3		Pin21 → Pins 29,30				
ton4		Pin19 → Pins 24,25				
toff1	Turn Off Delay Time	Pin17 → Pins 42,43	190	-	330	ns
toff2		Pin15 → Pins 40,41				
toff3		Pin21 → Pins 29,30				
toff4		Pin19 → Pins 24,25				
ICES1	Collector to Emitter Leakage current	Pins 2 to4 → Pins 42,43	-	-	200	uA
ICES2		Pins40,41 → Pins35to38				
ICES3		Pins29,30 → Pins 32,33				
ICES4		Pins24,25 → Pins 27,28				
IR1	Diode Leakage Current	Pins 32,33 → Pins 29,30	-	-	25	uA
IR2		Pins 27,28 → Pins 24,25				

TEST CIRCUIT 1

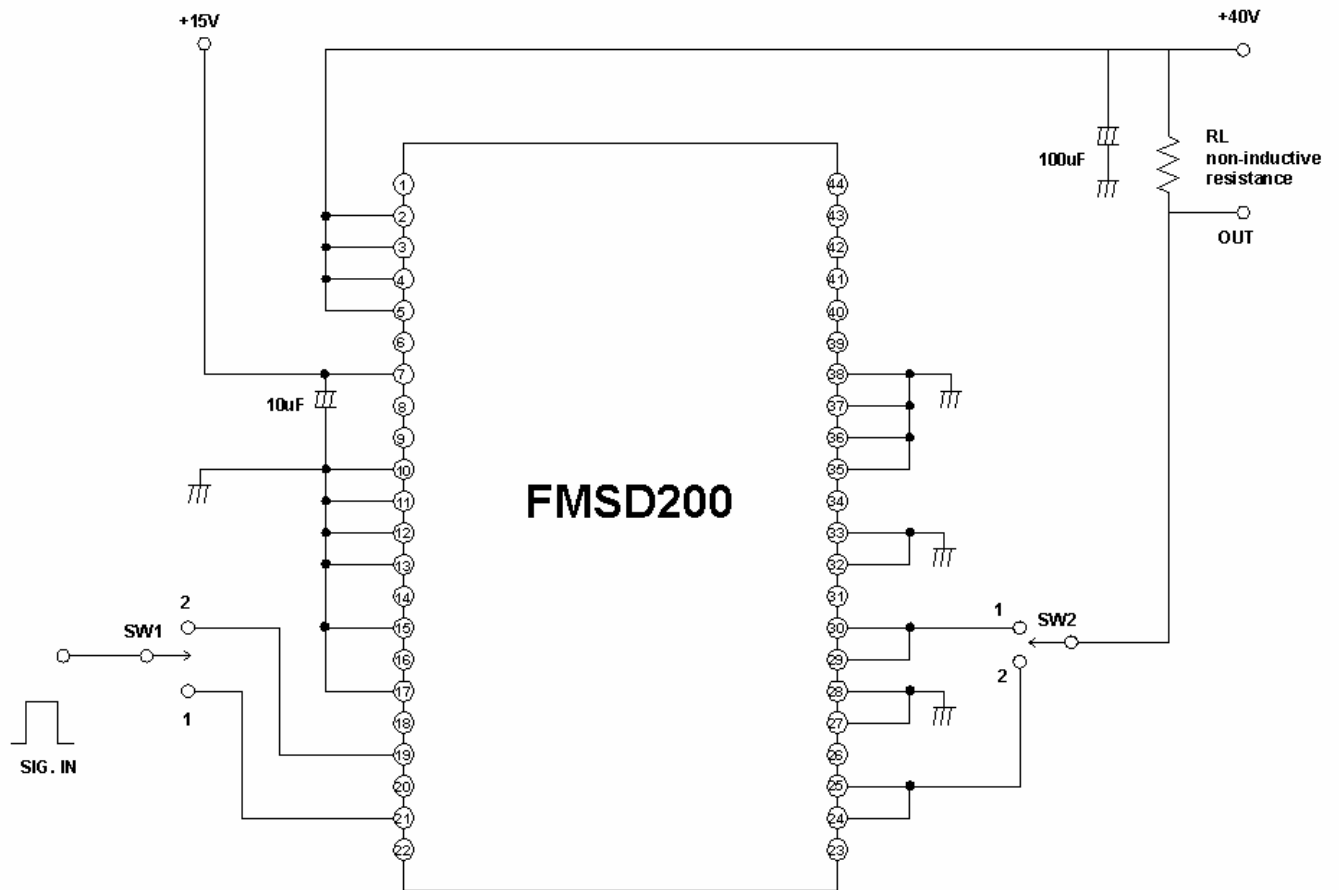


TEST Timing Chart :  $V_{IH}=5V$ ,  $V_{IL}=0V$

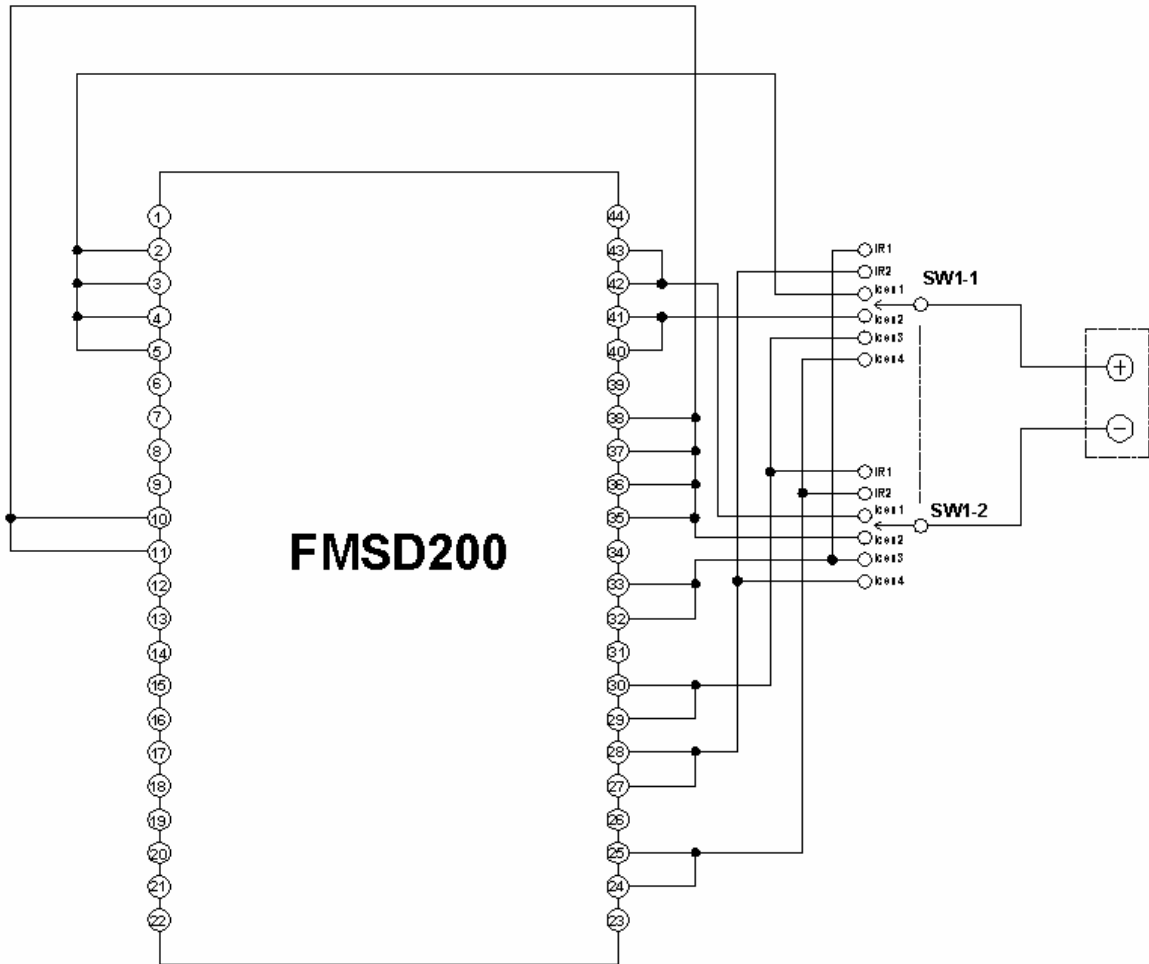


**TEST CIRCUIT 2**


Symbol	Contents of test	SW1	SW2	SW3	RL
Vsat	Output saturation voltage between pins 2 to 5 and pins 42,43	1	1	1	8Ω
Vsat	Output saturation voltage between pins 40,41 and pins 35 to 38	1	2	2	
td(on)1	Turn on delay time between pin 17 and pins 42,43	2	1	1	470Ω
td(on)2	Turn on delay time between pin 15 and pins 40,41	2	2	2	
td(off)1	Turn off delay time between pin 17 and pins 42,43	2	1	1	20Ω
to(off)2	Turn off delay time between pin 15 and pins 40,41	2	2	2	

**TEST CIRCUIT 3**


Symbol	Contents of test	SW1	SW2	RL
td(on)3	Turn on delay time between pin 21 and pins 29,30	1	1	470Ω
td(on)4	Turn on delay time between pin 19 and pins 24,25	2	2	
td(off)3	Turn off delay time between pin 21 and pins 29,30	1	1	20Ω
to(off)4	Turn off delay time between pin 19 and pins 24,25	2	2	

**TEST CIRCUIT 4**


Symbol	Contents of test	SW1	Voltage
IR1	Leakage current between pins 32,33 and pins 29,30	IR1	300V
IR2	Leakage current between pins 27,28 and pins 24,25	IR2	300V
Ices1	Leakage current between pins 2 to 5 and pins 42,43	Ices1	300V
Ices2	Leakage current between pins 40,41 and pins 35 to 38	Ices2	300V
Ices3	Leakage current between pins 29,30 and pins 32,33	Ices3	270V
Ices4	Leakage current between pins 24,25 and pins 27,28	Ices4	270V

**Package Dimensions** (dimensions in mm)

